Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended). A multiplier circuit with offset compensation, comprising:

an analog multiplier including a first signal input for receiving a first signal, a second signal input for receiving a second signal, and an output for providing a multiplied signal[[.]];

a first switching device for polarity reversal, said first switching device connected to said first signal input; and

a second switching device for polarity reversal, said second switching device connected to said second signal input.

Claim 2 (original). The multiplier circuit according to claim 1, wherein:

said first switching device includes a first clock input for receiving a clock signal;

and said second switching device includes a second clock input for receiving a clock signal; and

a clock signal having a changeover frequency is fed to said first clock input and said second clock input.

Claim 3 (currently amended). The multiplier circuit according to claim 2, wherein:

the first signal has a first frequency and the second signal has a second frequency; and

said changeover frequency is not less than two times a frequency selected from the group consisting of the first frequency of the first signal and the second frequency of the second signal.

Claim 4 (original). The multiplier circuit according to claim 3, wherein the changeover frequency lies in a range between 4 times and 32 times the largest frequency.

Claim 5 (original). The multiplier circuit according to claim 1, wherein the multiplied signal is a voltage that represents a product of the first signal and the second signal.

Claim 6 (currently amended). The multiplier circuit according to claim 1, wherein:

the first signal is a first differential signal and the second signal is a second differential signal;

said first signal input includes two terminals ~~for~~ each receiving the first differential signal; and

said second signal input includes two terminals ~~for~~ each receiving the second differential signal.

Claim 7 (currently amended). The multiplier circuit according to claim 6, wherein:

said first switching device includes a device for polarity reversal for reversing a polarity of the first input signal ~~that is~~ received by each of said two terminals of said first signal input; and

said second switching device includes a device for polarity reversal for reversing a polarity of the second input signal ~~that is~~ received by each of said two terminals of said second signal input.

Claim 8 (original). A quadricorrelator, comprising:

a first signal path;

a second signal path;

a first analog multiplier located in said first signal path, said first analog multiplier including an output and two inputs;

a second analog multiplier located in said second signal path, said second analog multiplier including an output and two inputs;

a differential node connected to said output of said first analog multiplier and to said output of said second analog multiplier;

a first switching device for periodically reversing a polarity of a signal selected from the group consisting of a quadrature component of a signal and a signal derived from the quadrature component of the signal and for thereby providing a first quadrature component signal, said first switching device connected to said two inputs of said first analog multiplier

for supplying the first quadrature component signal thereto; and

a second switching device for periodically reversing a polarity of a signal selected from the group consisting of another quadrature component of the signal and a signal derived from the other quadrature component of the signal and for thereby providing a second quadrature component signal, said second switching device connected to said two inputs of said second analog multiplier for supplying the second quadrature component signal thereto.